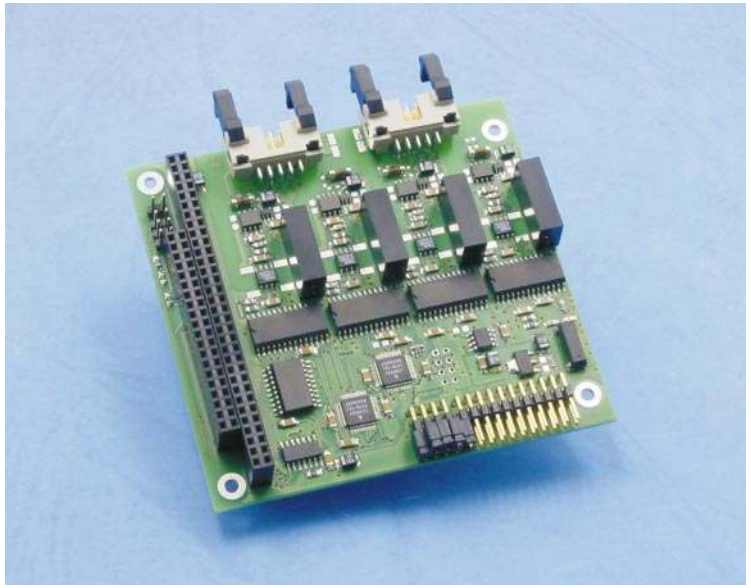

CAN-PC Interface

CPC-104M

User Manual

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Documentation for CAN-Interface CPC-104M.

Document version: 1.4
Documentation date: September 18th, 2008

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Our products are continuously improved. Due to this fact specifications may be changed at any time and without announcement.

WARNING: **CPC-104M hardware and software may not be used in applications where damage to life, health or private property may result from failures in or caused by these components.**

Contents

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1 Overview

1.1 Attributes

- CAN interface for industrial applications
- CiA DS 102 and ISO 11898 compatible physical layer
- Equipped with one to four NXP SJA1000 CAN controllers
- Galvanic decoupling between PC and CAN bus (optional)
- Easy programming based on direct mapping of CAN controller registers into PC memory area
- Automatic address range detection by memory managers

1.2 General Description

CPC-104M is a CAN interface module for PC-104 based systems. Designed for industrial series applications CPC-104M has a robust and cost efficient construction. CPC-104M supports up to 4 NXP SJA1000 CAN controllers.

CPC-104M maps the CAN controllers into the PC address space and thus allows access to CAN messages with low latency. Existing software for the supported CAN controllers can easily be adapted. With CPC-104M the CAN communication may be handled either in interrupt controlled or in polled mode, the interrupt channels 3–7, 9–12, 14 and 15 are available.

CPC-104M can optionally be delivered with galvanic decoupling to the CAN bus. In this case power for the DC/DC converter is derived from the +5V PC-104 line.

CPC-104M is available in different configurations regarding CAN channel count and galvanic decoupling.

Please refer to the “Ordering Information” section for more details. Configurations not listed may be available on request.

1.3 Ordering Information

Order Number	Description	Channel				CAN Potential			
		1	**2**	**3**	**4**	**1**	**2**	**3**	**4**
10-10-200-20	**CPC-104M/SJA1000S**	X	-	-	-	H	-	-	-
10-10-201-20	**CPC-104M/SJA1000S-GTI**	X	-	-	-	1	-	-	-
10-10-210-20	**CPC-104M/SJA1000D**	X	X	-	-	H	H	-	-
10-10-211-20	**CPC-104M/SJA1000D-GTI**	X	X	-	-	1-2	1-2	-	-
10-10-212-20	**CPC-104M/SJA1000D-GTIS**	X	X	-	-	1	2	-	-
10-10-230-20	**CPC-104M/SJA1000Q**	X	X	X	X	H	H	H	H
10-10-231-20	**CPC-104M/SJA1000Q-GTI**	X	X	X	X	1-4	1-4	1-4	1-4
10-10-232-20	**CPC-104M/SJA1000Q-GTIS**	X	X	X	X	1	2	3	4

H: Host potential
1, 2, 3, 4: Potential of CAN channel 1, 2, 3, 4
1-2; 1-4: Channel 1 and 2, 1 to 4 share potential

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2 Programming Interface

CPC-104M is mapped into the PC memory space at a base address in the area from C0000h to DE000h, occupies a range of 1536 Bytes and allows 8 bit accesses to its registers. The availability of the CAN controller registers in the memory area makes the CAN communication direct and provides a low latency time. The memory occupied by CPC-104M is divided into two subranges. The first subrange contains the configuration registers of the card and starts at the base address. The second subrange allows access to the CAN controllers and has 100h Bytes offset to the base address.

Address Offset	Description
0x000	Internal register
0x100	CAN controller 1
0x200	CAN controller 2
0x300	CAN controller 3
0x400	CAN controller 4

The configuration registers are described in the following table:

Address Offset	Access	Description
0	Read/ Write	Read: Constant 55h for card detection Write: Control register
1	Read	Constant AAh for card detection
2	Read	Encoding of occupied memory range in units of 512 Byte
3	Read	Constant CBh for card detection
4	Read	Identification of CAN controller constant 08h for SJA1000
6	Read	Status register
7	Read/ Write	Interrupt enable register
8	Read	Interrupt register
9	Read	CPLD Version

The status register contains the actual state of CPC-104M.The bits have the following meaning:

Status Register	
Bit	**Indication**
0	0: Hardware reset inactive at CAN controller 1: Hardware reset active at CAN controller
1	0: CAN controller unmapped into memory address range 1: CAN controller mapped into memory address range

Write accesses to the control register initiate actions within CPC-104M. The following table shows the transmitted data and the resulting action:

Control Register	
Value	**Function**
0	Hardware reset of CAN controller. A write of 0 generates a reset pulse of adequate length.
2	Unmap CAN controllers from memory address range.
3	Map CAN controllers into memory address range (write twice to take effect).

Initialization of the CAN controller and CAN communication are done by accesses to the

CAN controller registers. The register description may be taken from the data sheet of the NXP SJA1000 CAN controller.

Interrupt Register		
Bit	**Value**	**Description**
0	0	Interrupt of CAN 1 is inactive
	1	Interrupt of CAN 1 is active
1	0	Interrupt of CAN 2 is inactive
	1	Interrupt of CAN 2 is active
2	0	Interrupt of CAN 3 is inactive
	1	Interrupt of CAN 3 is active
3	0	Interrupt of CAN 4 is inactive
	1	Interrupt of CAN 3 is active
4:7	–	Reserved

Interrupt Enable Register (Write)		
Bit	**Value**	**Description**
1:0	10	Disable CAN 1 interrupt
	11	Enable CAN 1 interrupt
	00, 01	Command ignored
3:2	10	Disable CAN 2 interrupt
	11	Enable CAN 2 interrupt
	00, 01	Command ignored

Interrupt Enable Register (Write)		
Bit	**Value**	**Description**
5:4	10	Disable CAN 3 interrupt
	11	Enable CAN 3 interrupt
	00, 01	Command ignored
7:6	10	Disable CAN 4 interrupt
	11	Enable CAN 4 interrupt
	00, 01	Command ignored

Interrupt Enable Register (Read)		
Bit	**Value**	**Description**
1:0	00	Interrupt of CAN 1 is disabled
	01	Interrupt of CAN 1 is enabled
3:2	00	Interrupt of CAN 2 is disabled
	01	Interrupt of CAN 2 is enabled
5:4	00	Interrupt of CAN 3 is disabled
	01	Interrupt of CAN 3 is enabled
7:6	00	Interrupt of CAN 4 is disabled
	01	Interrupt of CAN 4 is enabled

Due to the board design the clock divider register (CDR) has to be initialized with 0x07 for BasicCAN or 0x87 for PeliCAN mode on **all** CAN controllers.

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3 Electrical Characteristics

3.1 Absolute Limiting Values

Any (also temporary) stress in excess of the limiting values may cause permanent damage on CPC-104M.

Parameter	Min	Max	Unit
Storage temperature	-40	85	°C
Operating temperature	-40	85	°C
Voltage on the bus connections	-30	30	V
Current across ground connection	-	1	A

3.2 Nominal Values

Parameter	Min	Typ	Max	Unit
Power supply on Pin B29 of the PC-104 connector	4,75	5	5,25	V
Current consumption on Pin B29 of the PC-104 connector*	-	250	-	mA
Voltage on bus pins**	-30	-	30	V
Clock frequency	-	16	-	MHz

* Measured with 80% bus load generated by a CPC-104M/SJA1000Q-GTIS at 1 MBit and nominal terminated bus lines.

** This voltage is measured against the ground potential of the CAN transceiver.

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4 Operating Instructions

4.1 Pin Configuration of CAN Connector

The CAN interface connector (D-Sub 9 male of the adapter cable) complies to CiA Standard DS 102. The pin usage is detailed in the following table:

Pin 1	–	Reserved by CiA
Pin 2	CAN_L	CAN_L bus line (dominant low)
Pin 3	GND	Ground
Pin 4	–	Reserved by CiA
Pin 5	–	Reserved by CiA
Pin 6	GND	Optional ground, internally connected to Pin 3
Pin 7	CAN_H	CAN_H bus line (dominant high)
Pin 8	–	Reserved by CiA
Pin 9	_	Reserved by CiA

4.2 Configuration

The configuration of the address space and the used interrupt channel is achieved by jumpers on CPC-104M. Their positions on the board is shown in figure 1.

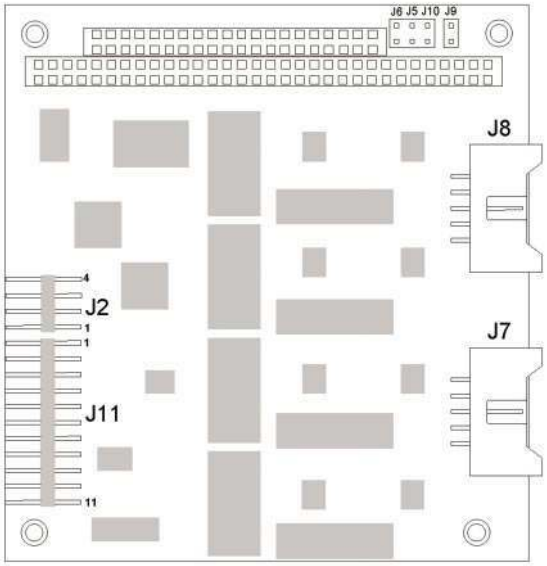

Figure 1: Jumper locations

The base address is set with jumper bank J2. The possible selections are listed in figure 2.

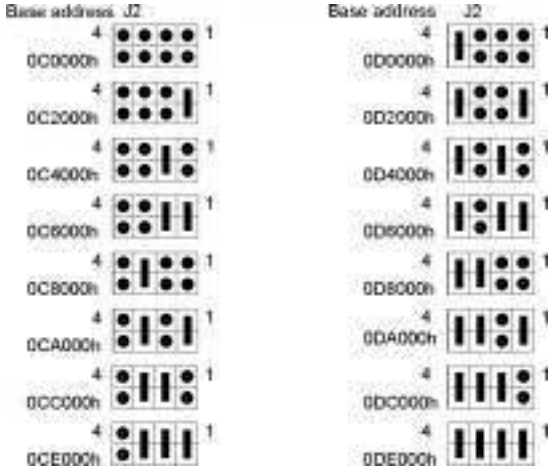

Figure 2: Selection of the memory base address

Jumper bank J11 determines the used interrupt channel. The settings can be seen in figure 3; the configuration for interrupt channel 5 is shown. It is not allowed to set more than one jumper on this bank.

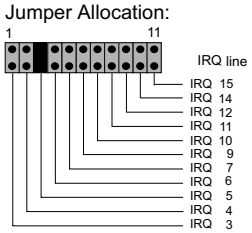

Figure 3: Interrupt settings

The following table shows the CAN Connector allocation:

Channel	Connector
1, 3	J7
2, 4	J8

4.3 Installation

CPC-104M may be installed in the board stack of a PC–104 system only. To avoid damage please pay attention to the following hints:

WARNING: Computer devices and components are sensitive against static discharge. For this reason keep CPC-104M in the antistatic cover until installing. Just before removing CPC-104M from the protection cover touch the metal case of your computer.

Avoid damage by achieving equal potential between all devices on the CAN before plugging the connection.

To the CAN adapter cable of CPC-104M only CAN networks with a connector and electrical characteristics complying with CiA DS–102 may be attached.

PC interface and CAN bus are not galvanic decoupled in the standard version of CPC-104M. Use in systems with diverging ground potential of PC and CAN bus is not permitted in this case.

Besides the instructions mentioned in this manual carefully observe the instructions in your computers users manual.

If you are not sure about the installation please contact **EMS Dr. Thomas Wünsche.**

Execute the following steps for installation:

- Disconnect your computer from the power line.
- Open the case of your computer and locate the correct position on the PC–104 stack.
- Plug CPC-104M carefully onto the PC–104 stack until it is completely seated.
- Fix CPC-104M with the proper mounting material
- Attach the adapter cable connector to an appropriate position in the computers case and close the case.